Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (cancelled)

Claim 2 (original) An integrator circuit comprising:

(a) an input conductor for conducting an input current;

(b) a first amplifier stage having an input coupled to the input conductor ;

(c) a second amplifier stage having an output and also having an input coupled to an output of the first amplifier stage;

(d) an integrating capacitor coupled between the input of the first amplifier stage and the output of the second amplifier stage; and

(e) an MOS compensation capacitor coupled between the input and output of the second amplifier stage.

Claim 3 (original) The integrator circuit of claim 2 wherein the first amplifier stage includes an input stage having an output coupled to an input of a folded cascode stage, an output of the folded cascode stage being coupled to a first terminal of the MOS capacitor, a second terminal of the MOS capacitor being coupled to the output of the second amplifier stage.

Claim 4 (original) The integrator circuit of claim 3 wherein the first and second amplifier stages co-act to establish bias voltage across the MOS capacitor so as to bias the MOS capacitor in its accumulation region for low values of the input current to provide a high value of compensation capacitance for the integrator

circuit and so as to bias the MOS capacitor in its inversion region for high values of the input current to provide a low value of compensation capacitance for the integrator circuit.

Claim 5 (original) The integrator circuit of claim 4 wherein the input current is a photodiode current containing a relatively low amount of noise for the low values of the input current and containing a higher amount of noise for the high values of the input current, and wherein an amount of noise produced by the integrator circuit when the value of the compensation capacitance is high is masked by the relatively high amount of noise.

Claim 6 (original) The integrator circuit of claim 2 wherein the first amplifier stage is a non-inverting amplifier stage and the second amplifier stage is an inverting amplifier stage.

Claim 7 (original) The integrator circuit of claim 2 wherein the MOS compensation capacitor includes an N-channel source region and an N-channel drain region both coupled to the input of the second stage amplifier, and also includes a gate disposed over a channel region between the N-channel source region and the N-channel drain region, the gate being coupled to the output of the second amplifier stage.

Claim 8 (original) The integrator circuit of claim 7 wherein the integrating capacitor is a poly capacitor.

Claim 9 (original) The integrator circuit of claim 2 wherein the input of the first amplifier stage conducts a single-ended input signal.

Claim 10 (original) The integrator circuit of claim 2 wherein the input of the first amplifier stage conducts a differential input signal.

Claim 11 (original) The integrator circuit of claim 6 wherein the second stage amplifier is an inverting class A amplifier.

Claim 12 (original) A CT scanner data acquisition system comprising:

(a) a plurality of integrator circuits, each including

i. an input conductor for conducting an input current,

ii. a first amplifier stage having an input coupled to the input conductor,

iii. a second amplifier stage having an output and also having an input coupled to an output of the first amplifier stage,

iv. an integrating capacitor coupled between the input of the first amplifier stage and the output of the second amplifier stage, and

v. an MOS compensation capacitor coupled between the input and output of the second amplifier stage;

(b) a plurality of photodiodes each having an anode coupled to an input conductor of an integrator circuit, respectively;

(c) a plurality of analog-to-digital converters, inputs of the analog-to-digital converters being coupled to the outputs of various integrator circuits.

Claim 13 (original) The CT scanner data acquisition system of claim 12 wherein the first amplifier stage includes an input stage having an output coupled to an input of a folded cascode stage, an output of the folded cascode stage being coupled to a first terminal of the MOS capacitor, a second terminal of the MOS capacitor being coupled to the output of the second amplifier stage.

Claim 14 (original) The CT scanner data acquisition system of claim 13 wherein the second amplifier stages co-act to establish bias voltage across the MOS capacitor so as to bias the MOS capacitor in its accumulation region for low values of the input current to provide a high value of compensation capacitance for the integrator circuit and so as to bias the MOS capacitor in its inversion region for high values of the input current to provide a low value of compensation capacitance for the integrator circuit.

Claim 15 (original) The integrator circuit of claim 14 wherein the input current is a photodiode current containing a relatively low amount of noise for the low values of the input current and containing a relatively high amount of noise for the high values of the input current, wherein an amount of noise produced by the integrator circuit when the value of the compensation capacitance is high is masked by the relatively high amount of noise.

Claim 16 (original) The CT scanner data acquisition system of claim 12 wherein the analog-to-digital converters are delta-sigma analog-to-digital converters.

Claim 17 (original) The CT scanner data acquisition system of claim 12 wherein the inputs of the analog-to-digital converters are coupled to common outputs of groups of the integrator circuits, respectively.

Claim 18 (original) The CT scanner data acquisition system of claim 12 wherein the first amplifier stage is an operational amplifier stage and the second amplifier stage is an inverting amplifier stage.

Claim 19 (original) The CT scanner data acquisition system of claim 12 wherein the MOS compensation capacitor includes an N-channel source region and an N-channel drain region both coupled to the input of the second stage amplifier, and also includes a gate disposed over a channel region between the N-channel source region and the N-channel drain region, the gate being coupled to the output of the second amplifier stage.

Claim 20 (original) The CT scanner data acquisition system of claim of 19 wherein the integrating capacitor is a poly capacitor.

Claim 21 (original) The CT scanner data acquisition system of claim 12 wherein the input of the first amplifier stage conducts a single-ended input signal.

Claim 22 (original) The CT scanner data acquisition system of claim 12 wherein the input of the first amplifier stage conducts a differential input signal.

Claim 23 (original) The CT scanner data acquisition system of claim 12 wherein the second stage amplifier is an inverting class A amplifier.

Claim 24 (cancelled)

Claim 25 (original) A method of operating an integrator circuit, comprising:

(a) conducting an input current into an input conductor of a first amplifier stage;

(b) coupling an input of a second amplifier stage to an output of the first amplifier stage;

(c) charging an integrating capacitor coupled between the input of the first amplifier stage and an output of the second amplifier stage; and

(e) compensating the integrator circuit by controlling the bandwidth of the integrator circuit by biasing an MOS compensation capacitor coupled between the input and output of the second amplifier stage into a predetermined operating region range.

Claim 26 (original) A method of operating a CT scanner data acquisition system, comprising:

(a) in each of a plurality of integrator circuits,

i. conducting an input current into an input conductor of a first amplifier stage,

ii. coupling an input of a second amplifier stage to an output of the first amplifier stage,

iii. charging an integrating capacitor coupled between the input of the first amplifier stage and an output of the second amplifier stage; and

iv. compensating the integrator circuit by controlling the bandwidth of the integrator circuit by biasing an MOS compensation capacitor coupled between

the input and output of the second amplifier stage into a predetermined operating region range;

(b) coupling an anode of each of a plurality of photodiodes to an input conductor of a group of integrator circuits, respectively;

(c) coupling inputs of a plurality of analog-to-digital converters to the outputs of various groups of integrator circuits, respectively.